Welcome

About DTIS 2017

On behalf of the Steering, Organizing and Program Committees, we would like to welcome you to the International Conference on Design and Technology of Integrated Systems in Nanoscale Era (DTIS) 2017, an event devoted to presenting and discussing scientific trends, emerging results, hot topics, and practical applications in the area of design and technology of integrated systems.

DTIS 2017 is the 12th edition of this conference and is held in Palma, Balearic Island, Spain.

Palma is renowned and valued as Europe's reference point for beach tourism, but it is also an ideal place for a millennial culture, and a lively and cosmopolitan city that makes an attractive destination 365 days-a-year. The city is the capital of Mallorca Island, located in the west part of the Mediterranean Sea. Palma offers a wide range of cultural, gastronomic, sporting and leisure options, making it especially attractive for enjoying a variety of experiences at any time of the year. Any visit to the city should include a tour of its most important historical buildings and its artistic heritage, its artistic patios, outstanding religious architecture and iconic buildings, as well as museums and art galleries.

The host of DTIS 2017 is the University of the Balearic Islands, founded in its current form in 1978 but with origins dating back to 1483, when King Ferdinand II of Aragon authorized the foundation of the Estudi General Lul·lià in Palma. This college and the building where DTIS takes place were named after the philosopher and writer Ramon Llull (c.1232–c.1315).

DTIS 2017 starts on Tuesday, April 4th and offers a three-day technical program, including 2 Keynotes, 6 Regular Paper Sessions, 3 Special Sessions and one Poster Session.

DTIS 2017 received a large number of contributions from all over the world. An electronic version of the formal proceedings has been included in an USB flash drive that has been distributed to conference attendees.

DTIS2017 is the achievement of the contributions by many volunteers, who give generously their time to contribute to the success of the symposium. We would like to thank all of them for their efforts.

We are confident that you will find DTIS 2017 a productive and exciting experience, and we would like to welcome you in Palma.

Miquel Roca & Eugeni Isern
DTIS 2017 General Chairs

Tiziana Margaria
DTIS 2017 Program Chair
Organizing Committees

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Arnaud Virazel  LIRMM
Xiaoqing Wen  Kyushu Institute of Technology
Murat Kaya Yapici  Sabanci University
Practical Information

Full program

This is the short program containing all relevant information in a compact manner. You can find the full program that also includes the full abstracts on the USB stick in your conference folder.

Conference venue

The DTIS 2017 conference takes place in Palma de Mallorca at “Sa Riera” building of the University of Balearic Islands placed in center town (street Miquel dels Sants Oliver, 2). Sessions will take place in the “Sala de Actos” (ground floor) and in room 22 (second floor), as it will be detailed later for each session.

“SA RIERA” building situation
Coffee breaks will be offered in the central yard (building ground floor) of the same building. Lunches will be served in the restaurant of the HM Jaume III Hotel, in Paseo Mallorca 14B, less than a 10 minute walk from the conference venue.

**Registration Desk**

The registration and information desk is open during the get-together as well as during the coffee breaks and the sessions. First day the desk will be placed near the main entry of the Sa Riera Building. For the remaining days the desk will move to the second floor.

**Guidelines for Speakers and Sessions Chairs**

The session room will be equipped with a laptop and a computer projector. Please be on time for your session and check in with your session chair. A volunteer or organizer will be available to set up your presentation and help you with any issues you might encounter. Presentations should emphasize the key issues and conclusions. Each speaker has in total 25 minutes for presentation and discussion, we propose to use at most 20 minutes for the presentation.

The chair coordinates the session. He/she introduces each presentation, informs the speaker when the time is running short and leads the discussion.

**WIFI Credentials**

Our university participates in the Eduroam initiative. Attendants coming from an institution that belongs to the Eduroam program can get connected to the “eduroam” wireless network. In order to get connected to this network, the credentials (username/password) served by the foreign institution must be used. It is important to use the user format that contains the domain of the institution (e.g. user@university.es).

Alternatively, we have set up a guest network for you, which can be used in the areas where the conference takes place. You should follow the next steps:

1. Connect to the Wi-Fi with SSID “eduroam” network.
2. Enter following username and password:
   
   *Username: dtis@wifi.uib.es*
   *Password: riera2017sa*

In case of problems associated with the previous network:

1. Connect to the Wi-Fi with SSID “uib@events” network.
2. Enter with the password “uib@events”.
3. Click on the 'Access for guests' option.
4. Enter the username and password.
Terms and conditions of use of the Wi-Fi user account:

- Anyone using the account must be somehow related to the meeting.
- The organization is responsible for any action taken from this service with this user account.
- The wrong usage of the network service will cause the definitive deactivation of the account in addition to the corresponding measures on the part of the Universitat de les Illes Balears

Conference Schedule

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Keynote speakers

Tuesday, 09:20-10:20

Dr. Jaume Segura. Universitat de les Illes Balears

“Integrated Microelectromechanical Systems in the More than Moore era”

Abstract
The classical IC integration roadmap has followed the Moore law for decades bringing up an impressive transistor scaling evolution resulting in a profound transformation of our quotidian practices. Current trends face the development of integrating multi-domain magnitudes within current systems, demanding a wider diversification of the parameters being managed and enabling what has been named as the More than Moore paradigm. The monolithic integration of such diversity of magnitudes is a challenge that will enable low-cost, highly complex personal systems. A view for the specific microelectromechanical domain will be shared.

Jaume Segura holds a degree in Physics from the University of the Balearic Islands (1989) and PhD in Electronic Engineering from the Polytechnic University of Catalonia (1992). He is currently full Professor at the University of the Balearic Islands where carries research within the Electronic Systems Group. His research interest is in the design, optimization and reliability of microelectronic circuits and MEMS / NEMS. He is co-author in more than one hundred research papers published in international journals and conference proceedings and holds five international (US) patents in conjunction with companies of the microelectronics industry. He has published two books with international editorialis (IEEE-John Wiley & Sons, SCI Tech-IET). He has conducted research stays at Philips Semiconductors USA, NM (USA) and has been visiting researcher at the Microprocessor Research Labs, Intel Corporation, OR (USA). He has lectured at Sandia National Labs (USA), AT & T Bell Labs (USA), Philips Semiconductors (USA), Intel Corporation (USA) among others. He has also taught courses in the framework of international conferences including the Design Automation and Test in Europe (DATE) Germany and the IEEE Int. Test Conf. (USA). He has been a member of technical and organizational committees of several international conferences such as IEEE Int. Test Conf., Design Automation and Test in Europe (DATE), IEEE VLSI Test Symposium, IEEE Int. On Line Test Symposium, IEEE European Test Symposium, and has been chairman of the Spanish chapter of IEEE-Circuits and Systems (IEEE-CAS) for eight years.
**Wednesday, 9:00-10:00**

**Dr. Michel Renovell, LIRMM Université de Montpellier**

**“Spot Defect Modeling: Past and Evolution”**

**Abstract**

With today manufacturing technology, it is not possible to eliminate all defects and ensure every manufactured unit is perfect. Instead, each manufactured unit must be tested so that defective parts are not shipped to a customer. Different Test Strategies are commonly used since none is considered as optimal in terms of low defect level. Most companies use some but not all of the following three Test Strategies: the Static Voltage strategy, the Dynamic Voltage or Delay strategy, the Static or Dynamic Current (I_DDX) strategy.

While using different approaches, these different test strategies have a common objective: reveal the presence in the chip of defects or deviations that may create a dysfunction.

Knowing the complexity of today defects, it is admitted that the classical fault models used for test generation cannot guarantee a satisfactory detection of defects.

This implies that new test generation technique specifically oriented to defects have to be defined. So, we must analyze and understand the electrical behavior of the defect and describe its behavior through an adequate ‘defect model’. Then, defect simulation techniques and defect-oriented ATPG techniques must be proposed to allow specific test generation for these defects.

This presentation focuses on spot defects that manifest themselves as shorts or opens in the interconnect or in the MOS transistors: ‘Interconnect open’, ‘Interconnect short’, ‘Floating gate’, and ‘Gate-Oxide-Short’ are analyzed in detail using different model levels.

For every defect, it is shown that the electrical behavior is in fact not predictable due to the presence of random parameters. In order to tackle the problem of unpredictability, unified concepts are proposed that allow new test generation techniques guaranteeing coverage of unpredictable defects.

Michel Renovell received his Ph.D. degree in applied physics in 1986 from the University of Montpellier, France. He joined the Laboratory of Computer Science, Automation and Microelectronics of Montpellier (LIRMM) in 1986 where he served as Head of the Microelectronics team from 2000 to 2005. He has been Deputy-Director of LIRMM from 2009 to 2016. He is also Scientific Delegate for the CNRS National Institute of Computer Science (INS2I) headquarter managing more than 50 French labs. He is author of more than 200 papers and member of the editorial board of JETTA and the VLSI Journal. He has been General Chair and Program Chair of a number of conferences (ETS, VTS, DDECS, DELTA, FPL, SBCCI, DCIS, DTIS…). He is IEEE Fellow for his contribution to defect based testing.
Program

Tuesday, 09:00-9:20  Opening Session (Salon de Actos Room)

Tuesday, 09:20-10:20
DTIS Keynote 1  (Salon de Actos Room)
Dr. Jaume Segura, “Integrated Microelectromechanical Systems in the More than Moore era”

Tuesday, 10:20-10:50  Coffee Break

Tuesday, 10:50-12:05
Session 1. IS Design 1  (Room 22, second floor)

Session chair: Michel Renovell (LIRMM, Université de Montpellier, France)

10:50 On Hammock Networks – Sixty Years After
United Arab Emirates Univ. (United Arab Emirates), “Aurel Vlaicu” Univ. of Arad (Romania)

11:15 Interconnect Networks for Resistive Computing Architectures
Hoang Anh Du Nguyen, Lei Xie, Jintao Yu, Mottaqiallah Taouil and Said Hamdioui.
Delft University of Technology (The Netherlands)

11:40 Run-time Resource Allocation for Embedded Multiprocessor System-on-Chip using Tree-based Design Space Exploration
Sima Sinaei, Andy Pimentel and Omid Fatemi.
University of Theran (Iran), University of Amsterdam (The Netherlands)

Tuesday, 12:05-12:55
Session 2: IS Technology 1 (Room 22, second floor)

Session chair: Ioannis Voyiatzis (TEI of Athens, Greece)

12:05 An Autozeroing Inverter Based Front-End for Resonating Sensors
Luca Marchetti, Yngvar Berg and Mehdi Azadmehr.
University College of Southeast Norway, University of Oslo (Norway)
12:30 Fabrication and Simulation of Electrically Reconfigurable Dual Metal-Gate Planar Field-Effect Transistors for Dopant-free CMOS
Tillmann Krauss, Frank Wessely and Udo Schwalke.
Technische Universität Darmstadt (Germany).

Tuesday, 12:55-15:00 Lunch Break

Tuesday, 15:00-16:40
Special Session 1. (Room 22, second floor)
System level design & development of secure applications with SEcube™

Session chairs: Giuseppe Airò Farulla - CINI & Politecnico di Torino, Anna-Lena Lamprecht - Lero, The Irish Software Research Centre, Johannes Neubauer - TU Dortmund

15:00 Holistic Security via Complex HW/SW Platforms
Giuseppe Airò Farulla, Paolo Prinetto, Antonio Varriale
Politecnico di Torino (Italy), Blu5 Labs Ltd (Malta).

15:25 Securing C/C++ Applications with a SEcube™-based Model-driven Approach
Frederik Gossen, Johannes Neubauer, Bernhard Steffen
University of Limerick (Ireland), TU Dortmund University (Germany).

15:50 Model Checking of Security Properties: A Case Study on Human-Robot Interaction Processes
Giuseppe Airò Farulla, Anna-Lena Lamprecht
Politecnico di Torino (Italy), Lero-University of Limerick (Ireland)

16:15 A fully Model-based Approach to the Design of the SEcube™ Community Web App
Steve Boßelmann, Dennis Kühn, Tiziana Margaria
TU Dortmund University (Germany), Lero-University of Limerick (Ireland)

Tuesday, 16:40-17:10 Coffee Break

Tuesday, 17:10-18:50
Session 3: IS Technology 2 (Room 22, second floor)

Session chair: Vicens Canals (Universitat Illes Balears, Spain)
17:10 Feasibility study of in-situ grown nanocrystalline graphene for humidity sensing
Dennis Noll and Udo Schwalke.
Technische Universität Darmstadt (Germany)

17:35 NANOcom: A Mosaic Approach For Nanoelectronics Circuit Design
Matteo Bollo, Giulia Santoro, Umberto Garlando and Maurizio Zamboni.
Politecnico di Torino (Italy)

18:00 Formal Analysis of Bandwidth Enhancement for High-Performance Active-Input Current Mirror
LIRMM-Université de Montpellier.

Gregory Provan.
University College Cork (Ireland)

Tuesday, 19:00-20:30 Welcome Cocktail (central yard)
**Wednesday, 09:00-10:00**

DTIS Keynote 2 (Room 22, second floor)
Dr. Michel Renovell “Spot Defect Modeling: Past and Evolution”

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**Wednesday, 10:00-10:40**

Poster Session. (Room 22, second floor)

Session chair: Tiziana Margaria (Lero-University of Limerick, Ireland)

**Soft-Error Detection in Register Files using Circular Scan**
Jan Schat
NXP Semiconductors (Germany)

**A method/approach leading to controlled randomization in validation of an IP**
Meghashyam Ashwathnarayan, Jayakrishna Guddeti
Infineon Technologies Private Ltd (India)

**A Global Approach for the Improvement of UHF RFID Safety and Security**
Rahma Ben Fraj, Vincent Beroulle, Nicolas Fourty, Aref Meddeb
University of Tunis (Tunisia), University of Grenoble (France), University of Sousse (Tunisia)

**On the Generation of Binary functions with Low-Overhead**
Ioannis Voyiatzis, C. Efstathiou
TEI of Athens (Greece).

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**Wednesday, 10:40-11:10 Coffee Break**

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**Wednesday, 11:10-12:50**

Special Session 2. (Room 22, second floor)
EDA challenges and solutions for revolutionizing healthcare

Session chairs: Prof. Graziano Pravadelli – Università di Verona, Italy
Prof. Daniela De Venuto – Politecnico di Bari, Italy

**11:10 Analyzing Ambient Assisted Living Solutions: A Research Perspective**
Ashalatha Kunnappilly, MDH, Vasteraas, Sweden
Axel Legay, INRIA, Rennes, France
Tiziana Margaria, Univ. Limerick and Lero, Limerick, Ireland
Cristina Secleeanu, Mälardalen University, Sweden
Bernhard Steffen, TU Dortmund, Germany
Louis-Marie Traonouez, INRIA, Rennes, France

11:35 Wearable Energy Harvesting: From Body to Battery
Michele Magno, ETH Zurich, Switzerland
David Boyle, Imperial College London, UK

12:00 Sound4All: Towards Affordable Large-Scale Hearing Screening
Nils Heitmann, Technical University of Munich, Germany
Philipp Kindt, Technical University of Munich, Germany
Thomas Rosner, PATH medical GmbH, Germany
Kapil Sikka, All India Institute of Medical Sciences, India
Amit Chirom, All India Institute of Medical Sciences, India
Dinesh Kalyanasundaram, Indian Institute of Technology, India
Samarjit Chakraborty, Technical University of Munich, Germany

12:25 A WBAN System for Quantitative Levodopa Effects Evaluation in Parkinson Disease by Jointly EEG-EMG Computing
Daniela De Venuto, Politecnico di Bari, Italy
Giovanni Mezzina, Politecnico di Bari, Italy

Wednesday, 12:50-15:00  Lunch Break

Wednesday, 15:00-16:15
Session 4: IS Testing & Validation (Room 22, second floor)

Session chair: Sebastià Bota (Universitat Illes Balears, Spain)

15:00 An Effective Fault-Injection Framework for Memory Reliability Enhancement Perspectives
Ghita Harcha, Alberto Bosio, Patrick Girard, Arnaud Virazel and Paolo Bernardi.
LIRMM-Université de Montpellier (France).

15:25 Processor-based Symmetric Transparent BIST
Ioannis Voyiatzis, C. Sgouropoulou
TEI of Athens (Greece)

15:50 Using Transition Fault Test Patterns for Cost Effective Offline Performance Estimation
Mahroo Zandrahimi, Philippe Debaud, Armand Castillejo and Zaid Al-Ars.
Delft University of Technology (The Netherlands), STMicroelectronics, Grenoble (France)
Wednesday, 16:15-17:30
Session 5: IS Technology 3 (Room 22, second floor)

Session chair: Jaume Verd (Universitat de les Illes Balears (Spain))

16:15 Evaluation of SRAM Cell Write Margin Metrics for lifetime Monitoring of BTI-induced Vth drift
Bartomeu Alorda-Ladaria and Gabriel Torrens
Universitat de les Illes Balears (Spain).

16:40 Oxide-based RRAM Models for Circuit Designers: A Comparative Analysis
Basma Hajri, Hassen Aziza, Mohammad Mansour and Ali Chehab.
American University of Beirut (Lebanon), Aix Marseille Université (France)

17:05 Cantilever NEMS Relay-Based SRAM Devices for Enhanced Reliability
Sebastià Bota, Jaume Verd, Joan Barceló, Xavier Gili, Tomeu Alorda, Gabriel Torrens, Carola De Benito and Jaume Segura.
Universitat de les Illes Balears (Spain).

Wednesday, 18:30-23:00 Social Event & Gala Dinner
Thursday, 9:30-11:00
Special Session 3. (Room 22, second floor)
Memristive Devices: Technology, Design Automation and Computing Frontiers

Session chairs: Mario Barbareschi (UNINA Italy), Alberto Bosio (LIRMM France), Ioana Vatajelu (TIMA France), Said Hamdioui (Delft University The Netherlands)

9:30 Memristive devices and their potential
Ioana Vatajelu, Grenoble Alpes University, TIMA Laboratory, France

10:00 Toward automation of memristive device based circuit design
Alberto Bosio, LIRMM, France

10:30 Memristive device based computing: Myth or reality?
Hoang Anh Du Nguyen, Delft University of Technology, The Netherlands

Thursday, 11:00-11:30 Coffee Break

Thursday, 11:30-12:45
Session 6: IS Design 2 (Room 22, second floor)

Session chair: Alberto Bosio (LIRMM, Université de Montpellier (France)

11:30 Synthesis tool for design of complex polymorphic circuits
Adam Crha, Richard Růžička and Václav Šimek.
Brno University of Technology (Czech Republic).

11:55 Compact Library of Efficient Polymorphic Gates based on Ambipolar Transistors
Jan Nevoral, Vaclav Simek and Richard Ruzicka.
Brno University of Technology (Czech Republic).

12:20 Analysis of two different charge injector candidates for an on-chip Floating Gate recharging system
Joan Cesari, Maria Del Mar Fernandez, Eugeni Isern, Miquel Roca, Salvatore Danzeca, Markus Brugger, Alessandro Masi, Eugenio García-Moreno and Álvaro Pineda.
IC-Málaga (Spain), CERN (Switzerland), Universitat Illes Balears (Spain)
Thursday, 12:45-13:00  Closing Session

Thursday, 13:00-15:00  Lunch Break
Social program

Tuesday, April 4 (19:00). Welcome Cocktail

A welcome cocktail will be served in the central yard (building ground floor) of the “Sa Riera” building -the conference venue-.

Wednesday, April 5 (18:30). City tour Palma

We will follow a guided walking tour to the most stunning spots in the city. The tour takes around one hour and a half. Departure is in front of the Conference Venue, and it will finish at the Restaurant “El Naútico”, where the gala dinner will be served.

Wednesday, April 5 (20:30). Gala dinner

The gala dinner will be held at “El Naútico”, (elnauticorestaurante.com) a charming restaurant looking at the Palma port and located in the Real Club Náutico of the city.
Contact persons

Eugeni Isern (eugeni.isern@uib.es)
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Margalida Homar (marga.homar@fueib.org)